Notice of Allowability	Application No.	Applicant(s)	
	10/787,347	KIMURA, HAJIME	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 01-26-07*.

2. ☒ The allowed claim(s) is/are *1,2,4,5,7-16,47-49,51,52 and 54*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 01-26-07
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *03-30-07* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and /or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST submit no later than the payment of the issued fee.

Authorization for this examiner' s amendment was given in a telephone interview with attorney Diana DiBerardino (Reg. No. 45,653).

The following changes have been made to the subject application:

In the claims

Cancel claims 17-46.

Reason for Allowance

The following is an examiner's statement of reasons for allowance: the prior art of records (US 2002/0008543) fails to teach or suggest a semiconductor device comprising: a transistor connected to a load; a first switch connected to the transistor; a second switch electrically connected to the transistor; first and second currents sources connected to the first and second switches for providing current through the source and drain of the transistor and for providing first and second potentials to the gate of the transistors as called for in claims 1, 2 and 4; a semiconductor device comprising a load, a constant current source, first and second transistors, a third switch connecting the gate to the drain of the first transistor and a fourth switch connecting the source to the drain of the second transistor as called for in claim 7; a driving method of a semiconductor device, comprising the steps of:
feeding a first current through a transistor via a first switch so that a gate terminal of the transistor has a first potential, feeding a second current through the transistor via a second switch so that the gate terminal of the transistor has a second potential, and feeding -a third current to a load through the transistor while the gate terminal of the transistor is kept at the second potential when the first switch and the second switch are turned off as called for in claim 47 ; a driving method of a semiconductor device comprising the steps of:
feeding a first current to a transistor through a first switch so that a gate terminal of the

transistor has a first potential, feeding a second current to the transistor through a second switch so that the gate terminal of the transistor has a second potential, and feeding a third current to a display element through the transistor while the gate terminal of the transistor is kept at the second potential when the first switch and the second switch are turned off as called for in claim 49 and a semiconductor device comprising: a load, a transistor electrically connected to the load a first switch, a first current source, a second current source; and a capacitor electrically connected to a gate terminal of the transistor, a source / drain terminal of the transistor is connected to the first current source and the second current source through a second switch, wherein the second current source feeds a first current to the transistor so that the gate terminal of the transistor has a first potential, and wherein the first current source feeds a second current to the transistor so that the gate terminal of the transistor has a second potential as called for in claim 51. Therefore, claims 1, 2, 4, 5, 7-16, 47-49, 51,52 and 54 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

03-30-07

TUAN T. LAM
PRIMARY EXAMINER